UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/042,924 | 01/09/2002 | Leonard Forbes | 303.684US2 | 5327 |

21186 7590 07/18/2003

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

| EXAMINER | |
|---|---|
| VESPERMAN, WILLIAM C | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | 4 |

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/042,924 | FORBES, LEONARD | |
| | Examiner | Art Unit | |
| | William C. Vesperman | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *7-35* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. This action is in response to applicant's filing of January 9, 2002.

### *Election/Restrictions*

2. This application contains claims directed to the following patentably distinct species of the claimed invention.

I. A method for forming an enhancement mode p-channel memory cell, comprising: forming an oxide layer of less than 50 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer; and forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer. (It appears that Claims 1 – 6 read on this species.)

II. A method for forming an enhancement mode p-channel transistor, comprising: forming an oxide layer of less than 50 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; and forming a floating gate on the oxide layer, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10 to the minus 7 Coulombs for longer than 1.0 hour at 20 degrees Celsius. (It appears that Claims 7 -11 read on this species.)

III. A method of forming a memory device, comprising: forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell

includes:forming an oxide layer of less than 50 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; and forming a floating gate on the oxide layer, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10 to the minus 17 Coulombs for longer than 1.0 hour at 20 degrees Celsius.; and forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells. (It appears that Claims 12 -17 read on this species.)

IV. A method for forming an enhancement mode p-channel transistor, comprising: forming an oxide layer of approximately 23 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; and forming a floating gate on the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10 to the minus 17 Coulombs for at least one second at 85 degrees Celsius. (It appears that Claims 18 - 20 read on this species.)

V. A method for forming an enhancement mode p-channel transistor, comprising: forming an oxide layer of approximately 23 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode pchannel transistor to

have an operating voltage of less than 2.5 Volts across the oxide layer.

(It appears that Claims 21 - 23 read on this species.)

VI. A method for forming an enhancement mode p-channel memory cell, comprising: forming an oxide layer of less than 50 Angstroms (Avon a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer; forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of approximately 10 to the 15 cycles over a lifetime of the enhancement mode p-channel memory cell. (It appears that Claims 24 – 26 read on this species.)

VII. A method for forming an enhancement mode p-channel memory cell, comprising: forming an oxide layer of less than 50 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer; forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of approximately 10 to the 12 cycles over a lifetime of the enhancement mode p-channel memory cell. (It appears that Claims 27 – 29 read on this species.)

VIII. A method for forming an enhancement mode p-channel memory cell,

comprising: forming an oxide layer of about 30 Angstroms (P,) on a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer; forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p channel transistor to have an operating voltage of about 3.0 Volts across the oxide layer. (It appears that Claims 30 – 32 read on this species.)

IX. A method of forming a memory device, comprising: forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell includes: forming an oxide layer of about 23 Angstroms (A) on a substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer forming a dielectric layer on the floating gate; and forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode pchannel transistor to have an operating voltage of approximately 1.0 Volts applied to the control gate; and forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.
(It appears that Claims 33 – 35 read on this species.)

3. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is

finally held to be allowable. Currently, Claim 1 is generic with regards to independent Claims 21 – 33.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. During a telephone conversation with David R. Cochran on July 10, 2003 a provisional election was made without traverse to prosecute the invention of Group I, Claims 1 - 6. Affirmation of this election must be made by applicant in replying to this

Office action. Claims 7 – 35 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. (US 6,008,091) in view of Tunneling Leakage Current in Ultrathin (less than 4 nm ) Nitride/Oxygen Stack Dielectrics, IEEE Electron Device Letters, Volume 19, No 10, October 1998, by Ying Shi, Xiewen Wang and T.P. Ma.

In regards to Claims 1 and 2, Gregor et al. teaches (Figure 1, Detailed Description, column 2, lines 45 - 51, columns 3 - 4 , lines 28 – 52) a method of forming an enhanced mode p-channel memory cell, comprising forming a thin silicon dioxide layer to allow tunneling of electrons between the floating gate and the substrate having a channel region separating a source and a drain region in the substrate; forming a floating gate on the oxide layer; and forming a dielectric layer comprising of a thin silicon dioxide capping layer ranging in thickness from 5 – 30 Angstroms on the floating gate; and forming a control gate on the dielectric layer.

Gregor et al. does not teach that the oxide layer is less than 50 Angstroms to allow tunneling of electrons between the floating gate and the substrate but teaches that the oxide layer is thin.

Ying Shi, Xiewen Wang and T.P. Ma teach using a ultra-thin nitride/oxide having a thickness less than 4 nm (40 Angstroms) and 2. 3 nm (23 Angstroms) see Figure 2 as per Claim 2, to replace silicon dioxide as the gate dielectric formed between the substrate and the gate in order to reduce tunneling leakage current and improve reliability.

Therefore, it would be obvious to modify the method of forming an enhanced mode p-channel memory cell as taught by Gregor et al. and incorporate a ultra-thin nitride/oxide having a thickness less than 4 nm to replace silicon dioxide as the gate dielectric formed between the substrate and the gate as taught by Ying Shi, Xiewen Wang and T.P. Ma, in order to reduce tunneling leakage current and improve reliability.

In regards to Claim 6, as detailed above, Claim 1 is unpatentable over Gregor et al. in view of Ying Shi, Xiewen Wang and T.P. Ma. Gregor et al. does not teach the further limitation of Claim 6. However, Ying Shi, Xiewen Wang and T.P. Ma teaches that the operating voltage should be less than 1.5 volts.

Therefore, it would be obvious to modify the method of forming an enhanced mode p-channel memory cell as taught by Gregor et al. and incorporate an operating voltage should less than 1.5 volts.as taught by Ying Shi, Xiewen Wang and T.P. Ma, in order to substantially reduce tunneling leakage current.

7. Claims 3, 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. (US 6,008,091) in view of Tunneling Leakage Current in Ultrathin (less than 4 nm ) Nitride/Oxygen Stack Dielectrics, IEEE Electron Device Letters, Volume 19, No 10, October 1998, by Ying Shi, Xiewen Wang and T.P. Ma and further in view of Sung (US 2001/0011744 A1).

In regards to Claim 5, Gregor et al. and Ying Shi, Xiewen Wang and T.P. Ma teach all the limitations of Claim1, but do not teach a floating gate which has a bottom surface in contact with the oxide area of approximately 10 to the minus 10 cm square.

Sung teaches (paragraph 0003) extremely small cavity sizes of less than a quarter micron.

Therefore, it would be obvious to modify the method of forming an enhanced mode p-channel memory cell as taught by Gregor et al. and Ying Shi, Xiewen Wang and T.P. Ma and incorporate extremely small cavity sizes of less than a quarter micron as taught by Sung in order to achieve faster processing speeds by reducing gate and channel dimensions. In addition, the continual reduction in gate and channel dimensions in order to increase the operating speed and capacity of the electronic memory devices is in alignment with Moore's Law involving continual reduction of electronic component dimensions over time.

In regards to Claims 3 and 4, Gregor et al., Ying Shi, Xiewen Wang and T.P. Ma and Sung teach all the limitations of the claims, except Ying Shi, Xiewen Wang and T.P. Ma and Sung do not teach a floating gate holding a charge of 10 to the minus 17

Coulombs. Gregor et al. teaches obtaining the holding charge using Equation (2) in meeting the further limitation of Claims 3 and 4.

. Equation (2) defines that the gate capacitance equals the dielectric constant of the insulating layer between the gate and the substrate divided by the thickness of the insulation layer (t) and multiplied by the bottom surface area (A) of the gate in contact with the insulation layer. Therefore, using a dielectric constant of 3.9 for the silicon dioxide insulation divided by the thickness of 23 nm or 2.3 times 10 to the minus 7 cm and a Farad conversion factor of 8.85 X 10 to the minus 14 F / cm and a bottom surface gate area of 10 to the minus 10 square centimeters, a holding charge of 10 to the minus 17 coulombs is determined for the floating gate. Using the applicant's admitted prior art and published data including Figures 6A and 6B providing an estimate of the temperature dependence and the dependence of retention time on gate tunneling oxide thickness as discussed in the applicant's specification (Pages 12 – 14), the floating gate's charge holding time at temperatures of 20 and 85 degrees Celsius is shown.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eltan (US 2002/0064911 A1) teaches a non-volatile electrically and programmable semiconductor memory cell using asymmetrical charge trapping. .

Forbes (US 2002/0020871 A1) teaches static NVRAM with ultra thin tunnel oxides.

Forbes (US 2002/0113262 A1) teaches static p-channel flash memory cells with ultra thin oxide layers.

Gosney, Jr. (US 3,882,469) teaches non-volatile variable threshold memory.

Hodges et al. (US 5,811,865) teaches forming an improved dielectric device.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

wcv

wcv

Art Unit 2813

July 13, 2003.

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800